

FORM PTO-1449 (MODIFIED)**LIST OF PUBLICATIONS FOR
APPLICANT'S INFORMATION
DISCLOSURE STATEMENT**

Applicant: Manjul Bhushan and Mark B. Ketchen
 Docket No.: YOR920030032US1
 Serial No.: Unassigned 10-023-249
 Filing Date: Concurrently Herewith
 Group: Unassigned 2826

U.S. PATENT DOCUMENTS

EXAMINER	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	FILING DATE IF APPROPRIATE
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FOREIGN PATENT DOCUMENTS

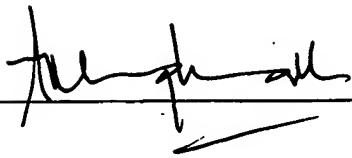
EXAMINER	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	TRANSLATION YES NO
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OTHER DOCUMENTS

EXAMINER	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
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NMD Taur et al., "Fundamentals of Modern VLSI Devices," 5.3 Sensitivity of CMOS Delay to Device Parameters, 5.3:1-4.3, pgs. 257-273 (1998).

Examiner



09/28/05

Date Considered

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.